Arbitrary Nanoscale Electrostatic Geometry via Localized h-BN Charge Trapping for 2D Quantum Transport

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June 19, 2026

Abstract

The realization of scalable quantum transport geometries requires atomically sharp, highly stable, and arbitrarily customizable electrostatic boundaries. While programmable ferroelectric architectures offer profound potential for non-destructive nanoscale gating, existing implementations are severely limited by instabilities in candidate materials. Organic ferroelectric copolymers, such as spin-coated P(VDF-TrFE), suffer from rapid polarization decay within 1–2 hours due to uncompensated internal depolarization fields, alongside severe remote impurity scattering from their amorphous matrices [1]. Concurrently, intrinsic van der Waals ferroelectrics are fundamentally limited by thermodynamic head-to-head domain wall broadening ($\sim$20–90 nm) in $\alpha - In_2Se_3$ [2] and catastrophic structural threshold switching driven by mobile Cu^+ ion migration in $CuInP_2S_6$ [3]. This proposal systematically addresses these fundamental limitations and presents a robust alternative: utilizing Conductive Atomic Force Microscopy (c-AFM) to inject stable, deep-level trapped charges into a single-crystal hexagonal boron nitride (h-BN) dielectric. By projecting floating gates onto channels in adjacent 2D materials, this lithography-free approach has potential to establish a highly stable and rewritable platform for low-temperature ballistic quantum transport without the structural or electronic disorder characteristic of ferroelectric gates.

Project Goals

Current state-of-the-art quantum device fabrication relies on physical etching or global gating architectures that require extensive, time consuming cleanroom processing that introduces permanent architecture. To bypass these limitations, this proposal establishes a generalized technique for drawing non-destructive, arbitrary electrostatic quantum boundaries using localized h-BN defect trapping. The specific goals of this research are:

Goal 1: Characterize and Calibrate h-BN Reading and Writing
Before defining complex quantum geometries, we will establish the spatial resolution limits and retention times of c-AFM localized charge injection in CVD-grown h-BN. By mapping injected charge gradients via Kelvin Probe Force Microscopy (KPFM) and testing thermal erasure cycles, we aim to build an empirical calibration matrix correlating applied tip potential to localized carrier density and lateral confinement width.

Goal 2: Realize Hard-Wall Hole Waveguides in WSe_2.
Utilizing our group's previously developed α-$RuCl_3$ charge-transfer architecture, we will achieve transparent, Ohmic contacts to monolayer WSe_2, preserving ultra-high hole mobilities ($> 80{,}000$ cm^2/Vs) [4]. By locally modulating the Fermi level deep into the valence band via targeted h-BN charge trapping

($n \approx 3 \times 10^{12}$ cm^{-2}), we calculate a Fermi level shift of $E_F \approx 10$ meV into the valence band, assuming a 2D hole gas with an effective mass of $m^{\approx}0.36m_e$ and lifted spin degeneracy ($g_s = 1$) and valley degeneracy ($g_v = 2$) at the K/K' valleys. We will define completely unetched, 1D ballistic waveguides bounded by the native 2.0 eV WSe_2 quasiparticle gap [5]. With this WSe_2 nanowire, we will benchmark the electrostatic confinement by probing for two hallmark signatures of phase-coherent transport: Fabry-Pérot charge-carrier interference [6] and conductance quantization [7]. To realize both phenomena, two distinct electrostatic geometries—a quantum cavity and a quantum point contact (QPC)—will be sequentially written and measured on the exact same device, explicitly demonstrating the non-destructive reprogrammability of the c-AFM technique.

Goal 3: Definition of a 1D Superconducting Wire in Magic-Angle Twisted Bilayer Graphene. This portion of the project will use a single device architecture pattern with the WSe_2 replaced with a magic angle twisted bilayer graphene (MATBG) sample. Utilizing non-destructive c-AFM local charge writing, we will first perform spatial transport mapping across the flake to locate the optimal twist-angle domain ($\theta \approx 1.1^\circ$). Once mapped, a 50nm wire will be defined in that region by drawing electron doped walls to confine transport by pushing the MATBG into an insulating regime [8]. By performing highly sensitive differential resistance (dV/dI) measurements across this single, reconfigurable architecture, we will systematically map the gate-tunable superconducting dome, quantify the critical current (I_c), probe conductivity quenching under high magnetic fields [9, 10], and track the emergence of finite-resistance tails driven by 1D quantum phase slips [11] in order to verify that the wire is superconducting and demonstrate the viability of c-AFM lithography for superconducting circuits.

1 Background and Scientific Motivation

Modern condensed matter physics increasingly focuses on exotic quantum states in highly sensitive 2D crystals. However, accessing these states often relies on conventional cleanroom lithography, an inherently violent process that degrades the pristine atomic order of these fragile materials. To overcome this, the field is rapidly shifting toward non-destructive, cleanroom-free device architectures that preserve the intrinsic quantum properties of the crystal. Among these are techniques that use scanning probes to slightly modify key components of devices while leaving the materials of interest completely untouched [12, 13]. Parallel efforts are completely rethinking device connectivity, replacing destructive deposited metals with van der Waals graphene contacts[14] and local ferroelectric gates [1] to preserve interface integrity. Both of these approaches, however, have key advantages and limitations. Though graphene contacts allow for highly ohmic contacts and noninvasive gates, they are difficult to use for gating configurations that only intend to bias specific points, and must be mechanically repositioned [15]. Ferroelectrics seek to solve that gating problem by placing a material that can freeze in a net electric dipole, maintaining a local gate with a simple bias from Piezoresponse Force Microscopy (PFM). This architecture has been realized using the organic ferroelectric copolymer P(VDF-TrFE) by Lv et al. [1], which allows for local polarization switching via Piezoresponse Force Microscopy (PFM). Concurrently, Wang et al. demonstrated that a molecularly thin, bistable monolayer electrolyte—cobalt crown ether phthalocyanine (CoCrPc) can achieve non-volatile, localized channel doping via Electric Force Microscopy (EFM)-driven ion manipulation [16]. While both strategies circumvent the structural damage of traditional lithography, they remain fundamentally ill-suited for defining the continuous, nanoscale potential landscapes required for fragile quantum transport. Amorphous polymer matrices like P(VDF-TrFE) introduce severe remote impurity scattering and suffer from rapid

polarization decay, while crystalline monolayer electrolytes are constrained by discrete, binary vertical ion configurations and molecular lattice quantization, creating a nonuniform potential landscape. Consequently, neither approach can encode the smooth, adiabatic electrostatic gradients necessary to suppress edge-state scattering in sub-micron channels. In this work I will address the fundamental limitations of current 2D crystalline ferroelectrics and propose the usage of Conductive Atomic Force Microscopy (c-AFM) to inject charges into defects of h-BN in order to create a tunable charge density for local gating that is robust at room temperature, easily customized in shape and size, and easily reprogrammable like a ferroelectric.

1.1 Limitations of 2D Ferroelectrics

To circumvent the electronic disorder introduced by amorphous organic polymers and molecularly discretized electrolytes, recent efforts have turned to intrinsic, crystalline two-dimensional van der Waals (vdW) ferroelectrics as an ideal platform for non-destructive, reprogrammable local gating. Because these crystals maintain structural crystallinity down to the monolayer or bilayer limit, they theoretically offer atomically smooth interfaces and high dielectric constants. However, when deployed as nanoscale gates for fragile quantum transport architectures, intrinsic 2D ferroelectrics exhibit severe thermodynamic and structural instabilities that fundamentally corrupt the definition of sharp potential boundaries.

Sliding Ferroelectrics (MoS_2,WTe_2, etc)

Sliding ferroelectrics are a frontier in ferroelectricity that utilize a unique interlayer sliding mechanism that can allow even semimetals like T_d-WTe_2 to exhibit ferroelectricity [17]. This process inherently presents itself as a challenge for clean, nanoscale quantum transport measurements. When locally poled via PFM, these materials tend to relax back to their original lattice configuration, overcome small switching barriers, or be pushed by local mechanical strain, representing an all-or-nothing switching function that is unfriendly to local writing on a scale smaller than the entire bilayer [18, 19, 20, 21].

$CuInP_2S_6$

To address these volatile domain issues in sliding systems, the same work by Sun et al. [18] presents Copper Indium Thiophosphate (CIPS) as a potential alternative for stable, easily writable domains. CIPS is a ferroelectric material that has mobile Cu^+ cations that reposition themselves within the crystal lattice on a per-unit-cell basis to create a ferroelectric effect down to a 4nm mechanical exfoliation limit [22]. In both cited papers on CIPS, PFM is employed to draw a box-in-box ferroelectric domain, which is the exact mechanism desirable for programmable gating. However, due to the mobile nature of the cations in the lattice, CIPS is also classified as a ferrionic material, meaning that the ions are readily mobile throughout the entire lattice when interacting with an external electric field [3]. In this paper by Zhong et al., it is recognized that there is an inherent difficulty in resolving the actual position of Cu^+ cations due to their tendency to migrate, leading to regions without ions present that are entirely unresponsive to PFM switching, heavily limiting the cleanliness of domain boundaries and making it difficult to arbitrarily place robust domains.

$\alpha - In_2Se_3$

To avoid the complications of long-range ion migration found in ferrionic systems like CIPS, recent work has turned to α-In_2Se_3. Originally predicted by Ding et al. to host intrinsic 2D ferroelectricity [23], α-In_2Se_3 behaves similarly to conventional 3D ferroelectrics, featuring a highly localized, bistable crystal structure that can be easily written and reconfigured via PFM. This structure also has another novel property, namely

a powerful in-plane polarization, which has proven useful in some ferroelectric field effect transistor architectures that employ this coupled nature to tune vertically stacked MoS_2 by two separate displacement fields [24]. However, when defining quantum scale edges, this in-plane ferroelectricity can cause unintended defects at domain boundaries. In a paper by Wang et al.[25], it is explored that the in-plane field causes incredibly blurry domain walls due to the amorphization of the phase of the indium selenide, introducing other crystal phases. These walls are pockets with zero ferroelectric order, which would cause massive issues if being used to gate, as the local band structure in stacked materials would be completely untouched at these walls, making precise modulation of metal-insulator transitions have undesirable shorts. Additionally, the domain boundaries tend to broaden on the order of 20-90 nm in order to maintain thermodynamic equilibrium. Even attempts to stack these domains vertically induce similar disorder, making the micro-level applications much less strong than the macro-level FET architectures [2].

1.2 Overcoming Ferroelectric Limitations via h-BN Defect Engineering

Upon close scrutiny, it is evident that ferroelectrics, though well suited to FET architectures, still fall behind permanent gating methods like graphene or metal deposition for quantum transport. However, the ideal local gating platform should not require sacrificing the reprogrammability of a scanning probe for the structural stability of a static gate. To bridge this gap, I propose exploiting the localized, deep-level defect states within hexagonal boron nitride (h-BN), the heavily studied, gold-standard dielectric of 2D device architecture.

Charge Trapping in Defect States of h-BN

While h-BN is often regarded as a pristine dielectric, its localized defect states have been recently highlighted as a source of unintentional electronic disorder in device performance. For instance, Lang et al. recently demonstrated that sliding dislocations within h-BN can trap substantial localized charge, generating stray potential barriers that directly impact the quality of transport in adjacent materials [26]. While their work notes that these specific macroscopic fault lines are largely suppressed in flakes thinner than 20 nm, it establishes an interesting premise: when filled with charge, intrinsic h-BN trap states act as robust, highly localized electrostatic gates that can be used to modulate adjacent materials. In order to explore this idea as a novel platform for intentional gating architectures, we must look toward native point defects in thin h-BN flakes which sit well below the threshold for fault line formation, and determine whether these local states can serve as a canvas upon which a robust, user-defined charge distribution can be written.

Engineering Defect Densities Suitable for Electrostatic Gating

Efforts in high-purity growth of h-BN crystals for 2D dielectric applications are the logical next step in this investigation, as defect concentration is well documented and highly dependent on synthesis techniques. Crystal growth methods for h-BN fall into two major categories that yield varying point defect densities. High-Pressure High-Temperature (HPHT) growth is the standard for high purity and is widely used for commercially available bulk crystals used in laboratory heterostructures. In a study by Onodera et al. [27], HPHT crystals are identified to possess two major macroscopic domains with differing defect concentrations. The pristine domains, typically occurring near the edges of the flakes, exhibit extremely low defect concentrations estimated at $\leq 10^{18}$ cm^{-3}, which sits at the operational limit of the optical noise floor. Conversely, the carbon-rich domains localized near the center of the exfoliated crystals host a higher defect concentration, spanning roughly 3×10^{18} to 10^{19} cm^{-3}. Taking a conservative concentration of $N_D \approx 3 \times 10^{18}$ cm^{-3}, we

can estimate the maximum programmable surface charge density (n_{hBN}) injected into a 10 nm thick flake of h-BN to be $n_{\text{hBN}} \approx 3 \times 10^{12}$ cm^{-2}. This represents a powerful induced surface charge. By deriving the geometric capacitance of the flake, we can calculate the effective gating potential (V_{eff}) generated by completely saturating these defects:

$$C_{\text{hBN}} = \frac{\varepsilon_0 \varepsilon_r}{d}$$

$$V_{\text{eff}} = \frac{e \cdot n_{\text{hBN}}}{C_{\text{hBN}}}$$

where e is the elementary charge, d is the flake thickness (10 nm), and $\varepsilon_r \approx 3.5$[28] is the relative permittivity of h-BN. This computation yields an effective local potential of approximately 1.55 V. This magnitude is more than adequate for local dual-gating geometries, confirming that defect charge trapping is physically robust enough to modulate quantum transport in adjacent materials.

However, as illustrated by Onodera et al., the fundamental drawback of utilizing HPHT crystals for local gating lies in this inherent domain segregation. The defect-heavy, carbon-rich domains are spatially restricted, relatively small, and unpredictably distributed throughout the exfoliated flake. Furthermore, locating these writable regions requires advanced cathodoluminescence (CL) spectroscopy prior to fabrication, which presents a severe and impractical bottleneck for rapid device engineering. More critically, if any continuous electrostatic gate were written across a boundary from a carbon-rich domain into a pristine domain, the trapped charge density would abruptly plummet, destroying the spatial uniformity of the potential barrier. In order to present a solution to this, we naturally turn to the other growth method, chemical vapor deposition (CVD). As shown by Zou et al.[29], CVD allows for direct tuning of defect density in order to engineer ideal substrates for specific applications. Another paper by Stewart et al.[30] also directly shows that the distribution of these defects is uniform throughout the CVD crystal, meaning that a substrate with a similar or even more defect dense h-BN flake could be produced in order to create an optimized maximum charge density. This tuning ability can be optimized by dissolving a small amount of carbon into the copper growth platform in order to add carbon substitutions into the lattice as shown by Tang et al.[31], where they achieved a density of 10^{14}cm^{-2}.

Electrostatic Carrier Injection and Trapping Mechanisms

With the programmable defect canvas established, the governing electrostatic and quantum transport mechanisms for localized charge injection must be defined. Driven by the extreme localized electric fields generated at the apex of a Conductive Atomic Force Microscopy (c-AFM) tip, carrier transport from the metallic probe into the wide-bandgap h-BN dielectric moves via Fowler-Nordheim (FN) tunneling. Under a large external potential, the electrostatic field severely bends the interfacial band structure, allowing electrons into the h-BN conduction band. Once injected, these hot carriers relax and become localized within the engineered point defects, forming the static gating potential. The exact voltage thresholds and layer dependencies of this tunneling mechanism were rigorously mapped by Lee et al. [32]. Their work demonstrates that for h-BN flakes four layers (≈ 1.38 nm) or thicker, low-bias direct tunneling is completely suppressed. This establishes a lower-bound geometric design rule for our proposed architecture: by utilizing CVD h-BN flakes exceeding this thickness threshold, the dielectric remains perfectly insulating under low-bias, allowing electrons to be injected into the upper lattice and relax into the defect sites without leaking through to the underlying conductor. Once localized, the stability of these charges depends on the thermal landscape.

As demonstrated by Nathawat et al. [33], charge escape in h-BN is governed by Poole-Frenkel thermal emission, heavily dependent on the surrounding thermal energy (k_BT) and the energetic depth of the trap state (E_{trap}). To quantify this stability, we look to density functional theory mappings of carbon substitutions in h-BN, which identify these impurities as acceptor levels residing roughly 1.0 to 2.0 eV within the bandgap [34]. By modeling the defect escape rate via the Arrhenius equation $P \propto e^{-\frac{E_{trap}}{k_BT}}$, we can project the operational charge retention time (τ) based on standard lattice attempt frequencies ($\nu_0 \approx 10^{13}$ Hz). This is a coarse estimate, and PF emission is also assisted by the local electric field of the charges, making a more conservative estimate on the timescale of weeks. Assuming a median trap depth of $E_{trap} \approx 1.5$ eV, this platform exhibits extreme non-volatile stability. At standard room temperature (300 K), the projected charge retention time exceeds 10^{12} seconds, preventing any spontaneous degradation of the written gate. Under the cryogenic conditions (< 4 K) required for advanced quantum transport measurements, carrier emission is completely suppressed, guaranteeing an indestructible, static electrostatic barrier during device operation. This exponential temperature dependence provides a rapid, built-in erasure mechanism. By globally elevating the substrate to standard annealing temperatures (600 K), the thermal energy (k_BT) overcomes the deep-level potential barriers, accelerating the emission rate by nearly thirteen orders of magnitude. Under these conditions, the trap retention time plummets to fractions of a second, rapidly flushing the localized electrons back into the conduction band. This thermal reset completely dissipates the electrostatic landscape without degrading the underlying h-BN crystal, establishing a fully reconfigurable canvas where complex nanoelectronic gating features can be written, evaluated, erased, and re-mapped on the same substrate, presenting the same flexibility as ferroelectric gates.

Additional Functionality of Charge Injection

A definitive advantage of localized defect trapping over both ferroelectric and metallic gating architectures is its ability to encode continuous, arbitrary electrostatic gradients. Ferroelectric gates are constrained by discrete polarization states, typically limited to binary except in select 3D materials, making them fundamentally incapable of encoding smooth lateral potential gradients. While conventional continuous metal gates allow for analog voltage modulation, their equipotential surfaces create spatially uniform field unless broken into highly complex, destructive multi-terminal arrays. Lassaline et al. [13] recently circumvented this limitation by using subtractive etching to pattern a sinusoidal thickness profile directly into an h-BN dielectric, creating a periodic potential gradient by spatially varying the local geometric capacitance. This physical approach, however, suffers from two critical drawbacks. First, the subtractive etching process introduces unavoidable structural disorder and surface roughness at the van der Waals interface, which could damage the pristine carrier mobilities required for quantum transport. Second, the etched gradient is mechanically permanent and cannot be reconfigured on a single device. The c-AFM charge injection method fundamentally circumvents both of these limitations. By dynamically modulating the c-AFM tip bias and dwell time during a spatial scan, a continuous areal carrier density gradient can be drawn onto a perfectly flat, unetched h-BN crystal. This purely electrostatic landscape remains fully reprogrammable, via global thermal annealing or localized, point-by-point opposite-polarity c-AFM overwriting for temperature-sensitive underlying channels.

2 Methodology and Experimental Design

2.1 Experiment 1 - Method Characterization and Calibration

To fabricate devices with high-quality electrostatic h-BN gates, the CVD crystals will be engineered to be approximately 10 nm thick, simultaneously avoiding direct tunneling through the crystal and suppressing transfer-induced fault lines. This experiment will include three main phases, organized by a logical chronological progression. The initial phase will act as a control, utilizing an independent 10 nm flake of h-BN transferred onto a blank SiO_2 substrate to test the gate injection method. To demonstrate bipolarity, both electron and hole injection will be performed, and the resulting localized domains will be imaged via Kelvin Probe Force Microscopy (KPFM). To explicitly map the write/erase cycle, the flake will be imaged (1) before injection, (2) after electron injection, (3) after thermal erasure to free the charge carriers, (4) after hole injection, and (5) finally after a second thermal erasure phase. Following this foundational validation, the h-BN canvas will undergo empirical calibration. First, to establish the fundamental spatial resolution limits, a high-resolution c-AFM probe (apex radius $\approx$ 10–20 nm) will be utilized to inject an isolated zero-dimensional point charge. High-resolution KPFM will map the resulting Gaussian potential profile, allowing us to extract the Full-Width at Half-Maximum (FWHM) and empirically define the lateral charge diffusion boundary. By subsequently patterning arrays of these point charges under varying tip biases, we will generate a precise calibration matrix mapping applied potential to localized carrier density. This calibration would enable highly localized writing by operating just marginally above the Fowler-Nordheim exponential tunneling threshold to actively suppress the lateral fringing of the injected charge, thereby maximizing boundary sharpness. Finally, this spatial calibration will be paired with continuous time-evolution monitoring in order to verify robust charge trapping. Simultaneously, repeated write/erase cycling will be conducted on a region of another flake to test the durability of these domains with repeated writing. Finally, the potential gradient will also be written similar to Lassaline et al. to show this capability.

2.2 Experiment 2 - 1D Quantum Channel Transport in WSe_2

Once writing is clearly mapped as a function of tip potential, a device will be constructed to verify the cleanliness of the boundary walls via quantum transport measurements. For this experiment, WSe_2 will be used as a semiconducting channel. Using a method developed by Pack et al. [4], high mobility $\alpha - RuCl_3$ contacts will be placed on either end of a piece of WSe_2, a global graphite back gate will be included to tune the global Fermi level, and the entire device will be encapsulated by a 10nm CVD h-BN flake. The c-AFM lithographed channel will include a first 50nm undoped channel with a ”dumbbell” shape. At the ends of the dumbbell where the contacts are placed, a charge gradient will be encoded above the contacts, consistent with Pack’s work on contact impedance. Finally, two regions of lower charge density will be inserted into the central wire past the charge gradient to act as the reflective mirrors that cause some electrons to interfere with one another. If the channel is successful, sweeping the global back gate to tune the channel carrier density, Fabry-Pérot interference with an oscillatory conductance plot should be observed when measured at 1.5K in a cryostat [6]. After this experiment, a second geometry will be written on the same flake with a narrower channel ($\approx$ 10-20nm) in order to do another low temperature measurement and search for 1D

conductance quantization [7].

2.3 Experiment 3 - Definition of a 1D Superconducting Wire Using Magic-Angle Twisted Bilayer Graphene

For the final experiment of this proposal, a heterostructure consisting of Magic-Angle Twisted Bilayer Graphene (MATBG), an intrinsic superconductor at low temperatures [9], will be constructed. This device will feature a global graphite back-gate, contacts at either end of the twisted graphene sample, and an unetched channel defined in a similar dumbbell geometry to the previous experiment. A major challenge in MATBG devices is the variation in twist angle throughout a single flake. To address this, the c-AFM will be used to directly locate and target homogeneous domains of $\theta \approx 1.1^{\circ}$. Once the ideal domain is located, c-AFM charge injection will be used to draw highly doped electrostatic walls. These trapped charges act as a potent localized top-gate, offsetting the local carrier density to explicitly push the wall regions into the correlated insulator phase [8]. This creates a robust, non-destructive electrostatic boundary, confining the supercurrent to a pristine 1D point contact. To fully characterize the superconducting nature of the wire, low-temperature (< 1 K) differential resistance (dV/dI) measurements will be performed to map the tunable superconducting dome. Additionally, we will quantify the critical current (I_c) as a function of perpendicular magnetic field [10]. We wil finally probe for the emergence of finite-resistance tails at base temperature, a signature of 1D quantum phase slips proposed by Bezryadin and Tinkham. [11].

3 Expected Outcomes and Risk Mitigation

Benchmark tests will aim to realize a near-field gating potential of $V_{eff} \approx 1.5V$ as calculated earlier. Additionally, our target for FWHM measurements of charge injection is an ideal lateral width of ¡ 50nm, alongside high room-temperature stability projected by Arrhenius modeling. Regarding risk mitigation, the primary technical challenge lies in lateral charge diffusion, which could broaden the electrostatic potential beyond the ballistic mean free path of the WSe2 channel. If confinement widths exceed these tolerances, the writing parameters (tip bias and dwell time) will be recalibrated marginally above the Fowler-Nordheim threshold to minimize fringing fields. Importantly, even if deep sub-micron confinement is unachievable, the platform remains highly viable for programmable mesoscopic gating, quantum dots, and local carrier density engineering. Furthermore, if MATBG twist-angle homogeneity proves too low for wire definition in Goal 3, the c-AFM writing technique will instead be benchmarked on standard rhombohedral trilayer graphene (rTG), which also hosts gate-tunable correlated states but with higher device yield. Finally, to prevent dielectric breakdown (estimated at 15V for a 10nm sample [35]) or mechanical strain from the c-AFM probe, intermittent-contact voltage pulsing can be utilized to preserve the h-BN surface quality.

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