Carrier Density and Temperature Control of Sliding Ferroelectricity in T_d-WTe_2

WYATT GARRETT

Thesis Proposal

WISCONSIN
UNIVERSITY OF WISCONSIN–MADISON

Department of Nuclear Engineering and Engineering Physics
University of Wisconsin–Madison

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Committee:
Daniel Rhodes, Professor, MS&E
Benedikt Geiger, Professor, NEEP

Contents

Abstract

T_d-WTe_2 is a semimetal that exhibits sliding ferroelectricity; however, systematic studies of how polarization and switching behavior evolve under varying carrier density, displacement field, and temperature conditions are limited. Trends and theoretical predictions imply a carrier density and temperature limit, both of which are not fully explored. By independently tuning carrier density and displacement field, I intend to extract the switching barrier, quantify how the barrier changes under differing conditions, and infer polarization from transport quantities like resistivity. These parameters will enable thorough mapping of the link between carrier doping and polarization, which will be useful in determining how charge carriers screen polarizing forces. However, in order to test the limits of carrier density, higher temperature measurements than the usual 350K will be required due to how temperature impacts Fermi-Dirac statistics in charge carriers. To address these issues, a second type of device will be constructed with platinum to ensure high temperature stability. Together, these experiments will give insight into fundamental mechanisms that dictate sliding ferroelectricity in a 2D metal, and guide further research into metallic ferroelectrics.

1 Motivation

For this project, we plan to validate theoretical predictions of sliding ferroelectric behavior by investigating upper limits of both carrier concentration and temperature. These regions have been previously unexplored and will give valuable insight into how charge carriers degrade sliding ferroelectrics and how temperature destroys ferroelectric order. 2D sliding ferroelectric materials are a relatively new field in research for applications such as nonvolatile memory design [1], charge-to-spin conversion for spintronic devices [2], and to enable the next generation of integrated circuits [3],[4]. Ferroelectric materials have the unique property of having an internal electric dipole that can be flipped between two states under an applied electric field. This switching forms a characteristic hysteresis loop that can be used in computer logic applications (Figure 1b).

A more recent development was the discovery of the aforementioned sliding ferroelectricity [3]. A prime example of sliding ferroelectricity is the subject of this paper, T_d-WTe_2, a transition metal dichalcogenide with a non-centrosymmetric van der Waals layered crystal structure (Figures 1c, 1d). Among other discoveries, T_d-WTe_2 has been shown to act as an insulator when exfoliated to a single layer. This remained previously unseen, as electrons that move freely in a metal are known to screen interlayer charge transfer, which is the dominant mechanism in ferroelectricity. This creates a ferroelectric in the normal direction that behaves as a conductor in the transverse directions, which has strong potential in electronics.

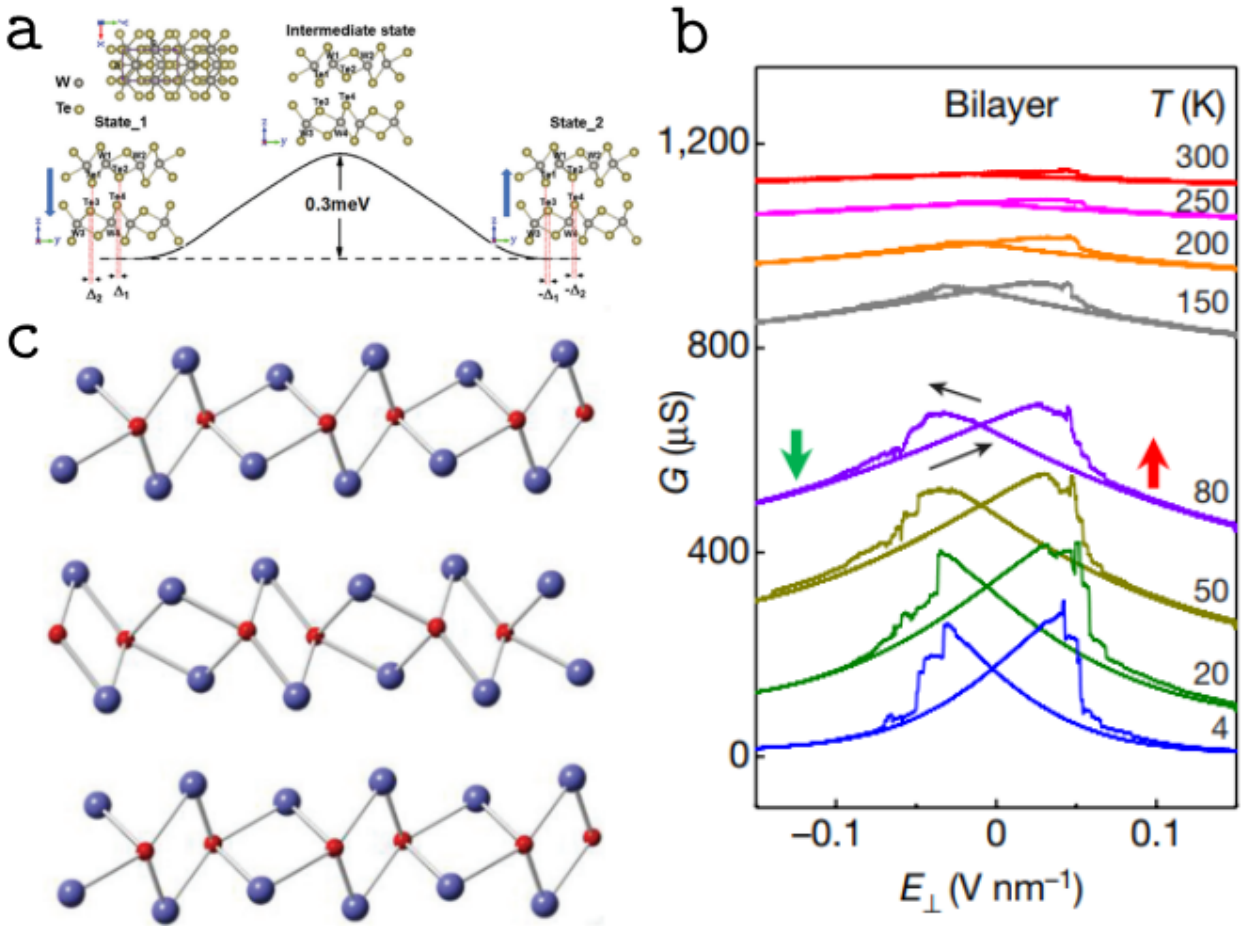

Figure 1: (a) Visual representation of sliding ferroelectricity depicting two stable states of polarization at either side of an energetic barrier formed by intermediate state [4]. (b) Plot of Conductance vs Longitudinal Electric Field showing hysteresis loop [5]. (c) schematic of T_d-WTe_2 along a-axis and c-axis respectively [10]

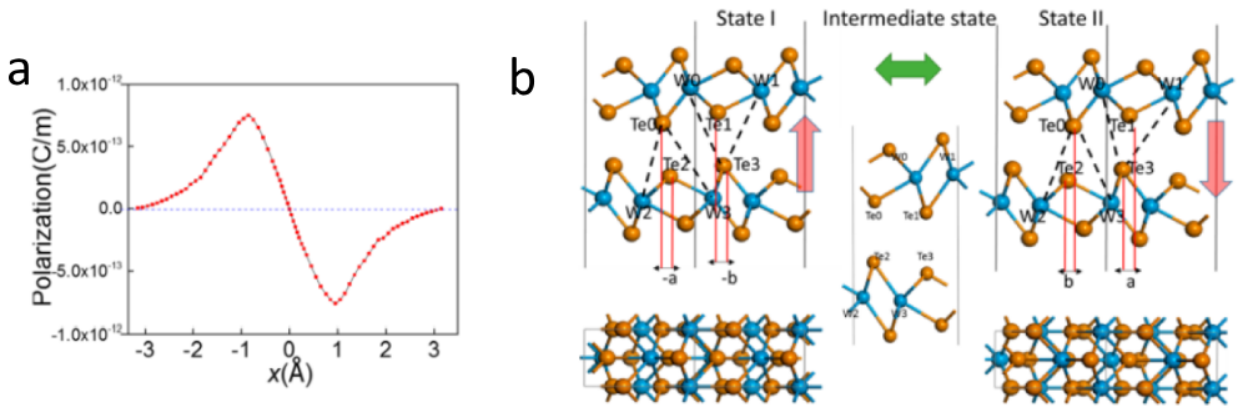

Figure 2: (a) Plot of electric polarization along switching direction. (b) Schematic of sliding ferroelectricity. [3]

2 Literature Review

2.1 Sliding Ferroelectricity in T_d-WTe_2

T_d-WTe_2 was first observed to be a ferroelectric in 2018[5]. This discovery led to investigations of ferroelectricity in other TMDs, including $MoTe_2$ [7], which also exhibits a superconducting phase simultaneously with the ferroelectric switching in its T'/T_d phase [8]. This class of materials has been observed to have a very small polarization switching barrier, with measured values of approximately 0.6-0.3 meV per unit cell.

This discovery was against conventional knowledge at the time, as the electrons that are free to translate in metallic solids were known to screen interatomic electrostatic forces which enable ferroelectricity [9]. Despite this uncertainty, hysteretic behavior was seen in the Fei paper, leading to a necessity for a structural framework that could explain the ferroelectricity. The same year as the Fei paper, Yang et al. [3] experimentally confirmed the sliding ferroelectricity in T_d-WTe_2 samples via Transmission Electron Microscopy (TEM). This paper examined the mechanism of ferroelectric polarization changes by showing two stable translational states. These positions were shown to correspond to the two polarization states and confirmed a new ferroelectric mechanism that was viable in metals.

2.2 Dependence of Ferroelectricity on Extrinsic Parameters

Sliding ferroelectricity has been shown to be dependent on multiple extrinsic parameters, including temperature, pressure, carrier density, and number of layers. Initial probing of T_d-

WTe_2 via Raman spectroscopy showed a total of 12 independent Raman modes in samples varying from 1 to 8 layers [10].There are also proposed mechanisms of ferroelectricity in tri- and five-layer samples [5].

Temperature, like in conventional ferroelectrics, is predicted to play a large role in sliding ferroelectrics [4]. The Curie Temperature is approximately where the ferroelectric behavior of the metal decomposes, reducing it to a paraelectric. This temperature is observed to be very sensitive to a variety of factors like switching barrier and carrier concentration[19]. However, in review of various publications, it is evident that this temperature is in a state of heavy uncertainty. The Tang paper theoretically estimates this value to be 660 K under ideal conditions through principles of condensed matter physics, while there are claims that the value is above 350 K, these are without any extensive probing past that limit due to hardware complications [5].

Another important extrinsic factor that would play a role on the mechanism of sliding ferroelectricity would be ambient pressure. In a paper by Liu et al. [11] in 2023, computations using Density Functional Theory showed a dependence of the potential barrier in the ferroelectric transition to be highly dependent on external pressure, likely coming from a smaller interlayer spacing. Pressure variation testing is beyond the intended scope of this proposal and all experiments will be carried out at ambient pressure.

The final factor that is important to this research will be the carrier density of the samples. There is a shown correlation between the relative electron and hole densities and the magnitude of the hysteresis loop[5]. The hysteretic behavior of samples are shown to degrade in high electron concentrations, but values above 8.8×10^{12} cm^{-2} are not probed and hysteretic behavior is still shown at this maximum.

2.3 Gaps in Current Literature

Though many papers do rigorous measurements of many different parameters like kinetics and field-driven switching, there appears to be a clear lack in some key experimental measurements that can motivate further theory. There currently exist no papers that independently study polarization and switching barrier as a function of carrier density. Fei. et al [5] paper demonstrated conductance based signatures of polarization switching and Bai et al. [12] carried this forward by doing experiments under different gating configurations and measured the kinetics of the sliding as a function of field through conductance changes. However, there is a lack of literature based on a swept measurement of polarization magnitude as a function of n as it approaches its limiting value. It would also be helpful to explore the magnitude of the switching barrier of the polarization change as a function of carrier density, as this would serve as a clear tunable parameter in device applications.

Another gap comes from measuring Hall resistivity in different polarization states. Conductance hysteresis plots show different peaks in opposing polarization states, however there is no clearly established formulation of why electron and hole dominated regimes conduct

asymmetrically. Mapping the dependence of both the xx and xy components of resistance on a Hall pattern as a function of carrier densities and polarities would fill this gap and give insight into how transport works differently in sliding ferroelectrics.

Curie temperature is another area of interest in devices, as operational temperatures play a massive role in potential device applications. Of the cited papers, experimental and theoretical ([5, 12, 19]), experiments have observed some polarization switching up to 350 K but with no further probing, and theoretical papers estimate 660 K under idealistic conditions. What is needed to better understand temperature dependence is a controlled and repeatable protocol for the determination of the Curie temperature. With an experimental protocol, I can then gather data up to critical temperatures and investigate these temperatures as a function of carrier density.

3 Approach

3.1 Device design

The design of the data collection device features a top and bottom gate both made of multilayer graphene (Gr) for the purpose of generating an electric field within the interior of the device. To ensure that there is as little current as possible inside of the device, two pieces of hexagonal boron nitride (hBN) are inserted between the gates as dielectrics. On top of the bottom hBN dielectric, an Au/Pd Hall measurement pattern will be deposited via lithography and vapor deposition. Finally, between the Au/Pd prepattern and top hBN dielectric, the T_d-WTe_2 sample will be stacked, creating a 6-layer device. The upper hBN flake will then be etched to expose the Hall contacts, and to those there will be gold wires bonded via silver paste in the low temperature device. The high temperature devices will substitute the gold Hall patterns with platinum to withstand temperatures higher than 350 K.

The fabrication steps will involve a mechanical exfoliation of each constituent material using Scotch tape exfoliation onto a Si/SiO_2 substrate. Following exfoliation and sample selection based on surface area and thickness, the bottom Gr and hBN samples will be stacked on a transfer stage using a PC transfer method in ambient conditions. Then the Hall pattern will be deposited using E-Beam Lithography and vapor deposition. The following steps are done in an argon glovebox. These steps include the exfoliation of the WTe_2 sample and the stacking of both the WTe_2 and the top hBN and Gr gate. A more detailed explanation of this process is in the supplemental information attached to the paper by Wang et al. [18].

3.2 Quantitative measurement techniques

The most important factors in the design of device and the measurements done is the thickness of samples, which will be verified using an Atomic Force Microscope (AFM). These measurements will allow for tuning of measured values from the 6-Probe Hall pattern on the device by determining sample thickness. It will also allow for determination of dielectric

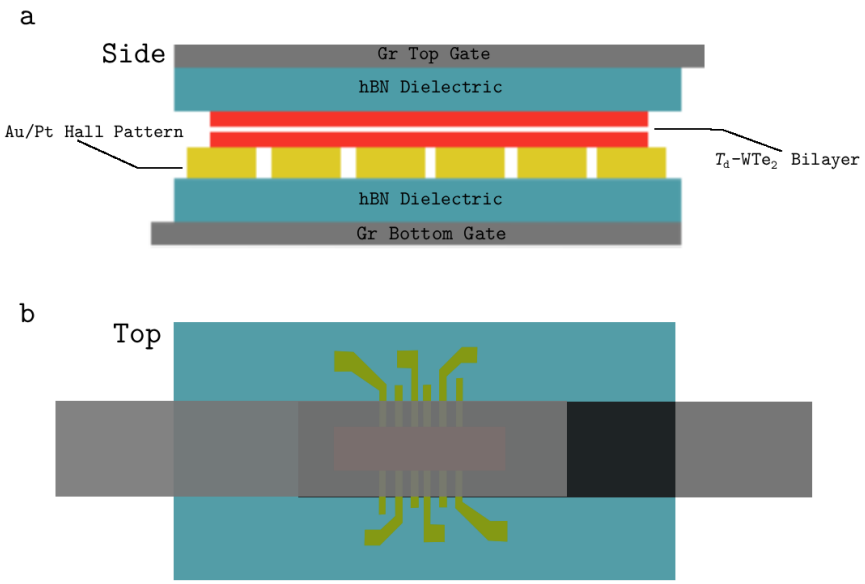

Figure 3: Schematic of device to be constructed with labeled material components, from a a) Side View and b) Top View

thicknesses, helping to get the capacitance across them and disentangle the carrier density and displacement field through the dual gate method.

Once the dimensions of all gates, dielectrics, and the sample itself are measured, the data can be used within Hall calculations and the capacitances across the dielectrics can be calculated from the parallel plate capacitance relation $C = \epsilon_r \epsilon_0 \frac{A}{t}$ with ϵ_r being the relative permittivity and t being the dielectric thickness. The terms in the matrix that relates the top and bottom gate voltage to the carrier concentration and displacement field are related to the dielectric capacitance by the link between capacitance and charge density by

$$\Delta n = \epsilon_0 \epsilon_{hBN} \frac{V_{TG}/d_{TG} + V_{BG}/d_{TG}}{e}, \tag{1}$$

$$\Delta D = \epsilon_{hBN} \frac{V_{TG}/d_{TG} - V_{BG}/d_{BG}}{2}. \tag{2}$$

$$\begin{bmatrix} n \\ D \end{bmatrix} = \begin{bmatrix} \frac{\epsilon_0 \epsilon_{hBN}}{e d_{TG}} & \frac{\epsilon_0 \epsilon_{hBN}}{e d_{BG}} \\ \frac{\epsilon_{hBN}}{2 d_{TG}} & -\frac{\epsilon_{hBN}}{2 d_{BG}} \end{bmatrix} \begin{bmatrix} V_{TG} \\ V_{BG} \end{bmatrix}. \tag{3}$$

$$\begin{bmatrix} n \\ D \end{bmatrix} = M \begin{bmatrix} V_{TG} \\ V_{BG} \end{bmatrix}, \quad M = \begin{bmatrix} \frac{\epsilon_0 \epsilon_{hBN}}{e d_{TG}} & \frac{\epsilon_0 \epsilon_{hBN}}{e d_{BG}} \\ \frac{\epsilon_{hBN}}{2 d_{TG}} & -\frac{\epsilon_{hBN}}{2 d_{BG}} \end{bmatrix}. \tag{4}$$

These equations come from Gauss's Law and parallel plate capacitance, where hBN is a linear dielectric, WTe_2 is a 2D conducting sheet, and voltages are with respect to the sheet

voltage of the WTe_2.

4 Proposed Research

4.1 What are the Limits of Polarization as a Function of Carrier Concentration and How is This Behavior Quantified

The objective of this study is to comprehensively map the polarization response of the sample and the free energy barrier to switching (Δ) as a function of both carrier density (n) and displacement field (D). From previous experimental studies, increasing carrier densities reduce hysteretic behavior of samples. In order to tune these parameters independently, a dual gate device will be used, introducing two potentials. Though the potentials will affect both n and D, the inclusion of two independent parameters allows the derivation of normal coordinates that only tune either carrier concentration or displacement field by the relation in equation (4).

Using measurements of capacitances across the top, C_T, and bottom, C_B, dielectrics as well as a term for the capacitance that penetrates the sample C_P. These can be used to extract the change in capacitance across the hysteretic regions, as seen in [22], which is then integrated with respect to carrier concentration to obtain $\Delta P(n, D)$ up to an additive constant. Using a reference point where the polarization is known to vanish, like in high carrier concentration, this can extract a strong polarization model.

Conductance hysteresis seems to disappear above a carrier concentration of $n = 10^{13}\text{cm}^{-2}$ in the Fei paper, so I expect to see zero polarization around the 10^{14}cm^{-2} carrier density regime. Understanding where this breakdown occurs will allow for determination of the constant and allow for the extraction of a relative polarization model as a function of carrier density.

4.2 How Does Resistivity Differ in Changing Polarization States

The Hall pattern on the proposed device will allow the determination of longitudinal and Hall resistances of the samples, allowing for a comprehensive mapping of carrier mobility in T_d-WTe_2. Using quantities measured by atomic force microscopy, we will be able to get constants and carry out resistivity testing. Using data from polarization in the previous section, We will be able to map how resistivity evolves as a function of polarization. We will also be able to fix a polarization magnitude and isolate carrier density measurements to gather control data of resistivity as a function of n alone. This will allow for quantification of how polarity directly impacts resistivity and construction of a more accurate conductivity model in a polar metal.

A major advantage of Hall measurements in this case is that the longitudinal and trans-

verse conductivity measurements allow for the extraction of a conductivity tensor. There is evidence of changing polarity in the y-axis without a polarization switch [3]. This change in magnitude is relatively small, however it does appear to serve as an additional polarity tuning parameter on a lower order of precision. This w

4.3 Gathering Data for Curie Temperature in T_d-WTe_2

Curie temperature of T_d-WTe_2 is a measurement that is not formalized experimentally, and one which could very heavily impact some of the measurements earlier referenced in this study. By the relation in Tang and Bauer [19], the coercive field has scaling factor dependent the Curie temperature via a Curie-Weiss power law relation. Being able to quantify T_c would, among other applications, give a better picture of switching barrier.

$$E_C(T, \Delta) = -\frac{8\Delta}{3\sqrt{3}P_0}(1 - \frac{3\gamma}{\sqrt{\pi}})^{3/2}(1 - \frac{T}{T_C})^{\eta} \tag{5}$$

The formula suggests that ferroelectric behavior ceases at the Curie temperature, similar to in ferromagnets. Switching behavior can be quantified by observing a magnitude switch in polarization, meaning that a similar device to the one used in previous measurements will suffice, just with the aforementioned temperature stability changes (section 3). Once at each incremental temperature, a simple gated polarization measurement will be conducted, looking for indications of switching. Once a temperature is verified, I will also measure it at different carrier concentrations, allowing for the construction of a ferroelectric T-n phase diagram.

5 Research Goals

The main goal of this project is to help inform a more comprehensive picture of energy transfer and electrical transport in sliding ferroelectrics. This will be accomplished by sequentially tuning parameters to gather many vital properties and mathematical dependencies that have not been explored directly previously, like polarization as a function of carrier density and rigorous Curie temperature. With some material dependent quantities verified, researchers will be able to use these trends to study other verified sliding ferroelectrics and use this intuition to design novel materials that optimize different conducting states and potential multiferroicity.

6 Material Needs and Cost

For this project, the required equipment will be growths of hBN, T_d-WTe_2, and Gr, which are all being constantly made in the Rhodes Lab. Additionally, gold and platinum wires will be used for the transport measurements, which are also present in the lab. Cleanroom work will also be done, and at the Engineering Centers Building costs $20 per hour of use time for a graduate student to do this, however this is already worked into the group's budget and will incur no extra cost beyond what is planned for. Within the clean room the pattern will

be deposited via E-beam lithography and vapor deposition, which are both included in the cleanroom budget. Low temperature measurements and AFM will be done within Rhodes Lab. This project is well within the regular lab operation and will require no additional external communication.

7 Expected Outcomes

In summary, this project seeks to build high resolution, quantitative measurements of important electrical parameters as a function of carrier density, displacement field, and temperature. Finding numerical values of breakdown temperatures and critical carrier densities will help to understand how these important tuning parameters affect sliding ferroelectrics. T_d-WTe_2 is the perfect candidate for this study as there is already proof of sliding ferroelectricity, general trends in directions, and deep understanding of the spatial geometry. Understanding T_d-WTe_2 at critical parameters will help us understand exactly how metallicity interplays with sliding ferroelectricity and pave the way for creating novel metallic ferroelectric materials like 2D multiferroics and superconducting qubits by tuning conducting states based on polarization.

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